

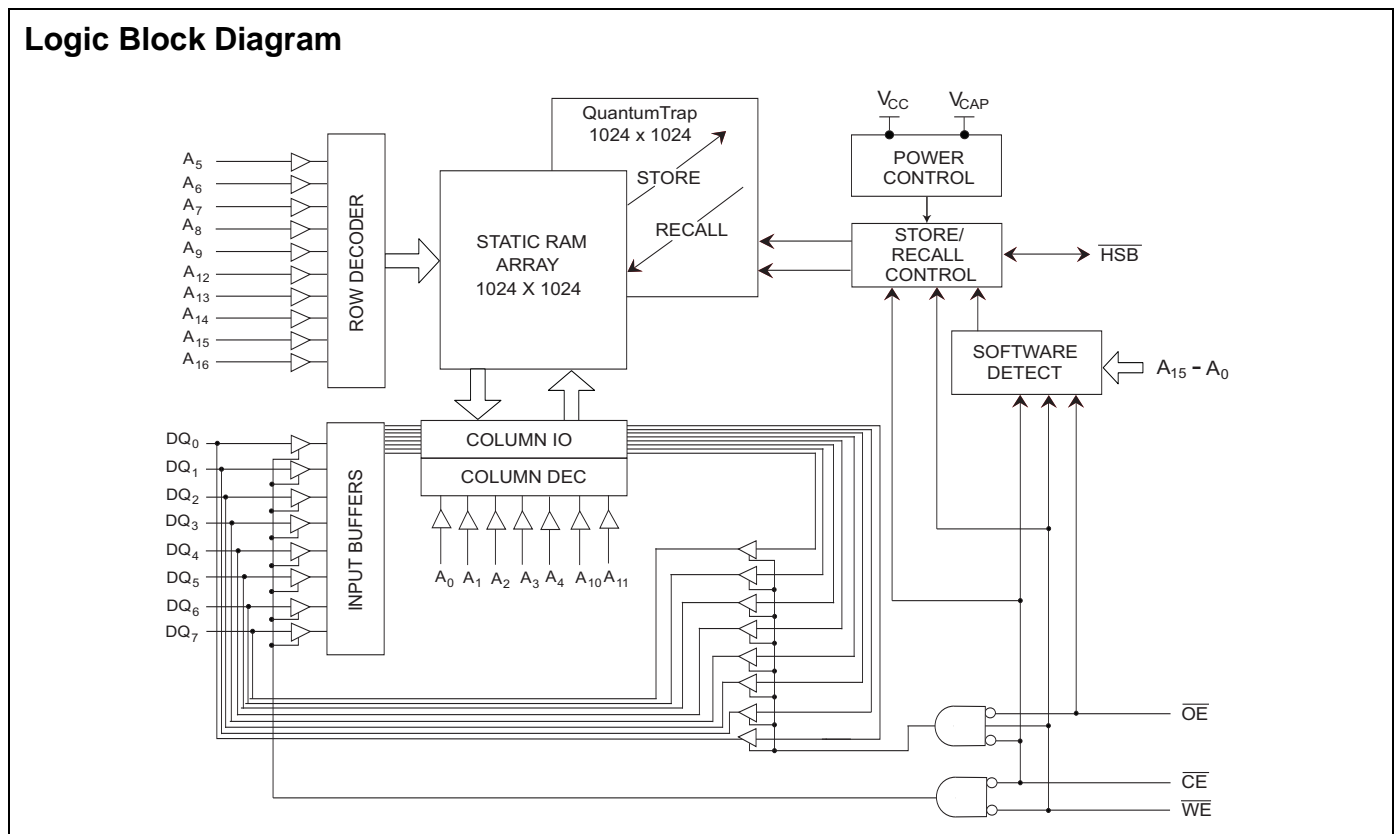
Features

- 25 ns, 35 ns, and 45 ns access times
- Hands off automatic STORE on power down with only a small capacitor
- STORE to QuantumTrap™ nonvolatile elements is initiated by software, device pin, or Autostore™ on power down
- RECALL to SRAM initiated by software or power up
- Infinite READ, WRITE, and RECALL cycles
- 10 mA typical I_{CC} at 200 ns cycle time
- 200, 000 STORE cycles to QuantumTrap
- 20 year data retention at 55°C
- Single 3V operation +20%, -10%
- Commercial and industrial temperature
- SOIC and SSOP packages
- RoHS compliance

Functional Description

The Cypress CY14B101L is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology, producing the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while independent, nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - 32-Pin SOIC

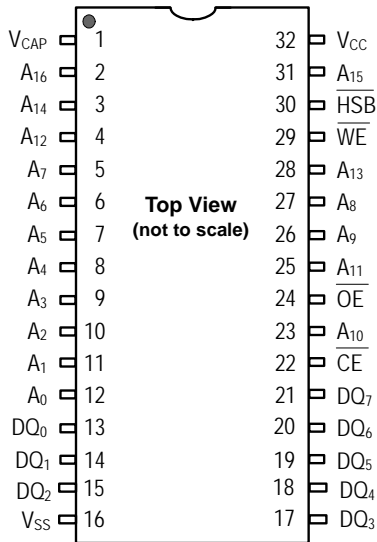


Figure 2. Pin Diagram - 48-Pin SSOP

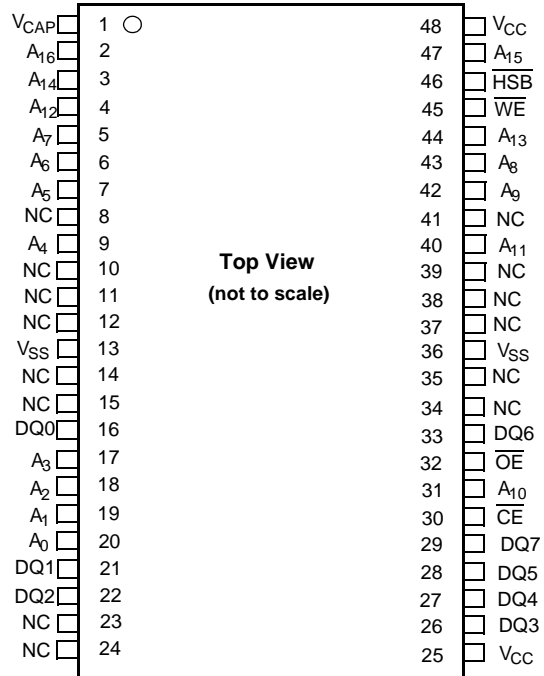


Table 1. Pin Definitions

Pin Name	IO Type	Description
A ₀ – A ₁₆	Input	Address Inputs. Used to select one of the 131,072 bytes of the nvSRAM.
DQ ₀ – DQ ₇	Input/Output	Bidirectional Data IO Lines. Used as input or output lines, depending on operation.
\overline{WE}	Input	Write Enable Input, Active LOW. When selected LOW, data on the IO pins is written to the address location latched by the falling edge of \overline{CE} .
\overline{CE}	Input	Chip Enable Input, Active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
\overline{OE}	Input	Output Enable, Active LOW. The active LOW \overline{OE} input enables the data output buffers during read cycles. IO pins are tri-stated on deasserting OE high.
V _{SS}	Ground	Ground for the Device. Must be connected to ground of the system.
V _{CC}	Power Supply	Power Supply Inputs to the Device
\overline{HSB}	Input/Output	Hardware Store Busy (HSB). When low, this output indicates a hardware store is in progress. When pulled low external to the chip, it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin HIGH if not connected. (connection optional)
V _{CAP}	Power Supply	AutoStore Capacitor. Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.
NC	No Connect	No Connect. This pin is not connected to the die.

Device Operation

The CY14B101L nvSRAM is made up of two functional components paired in the same physical cell, the SRAM memory cell, and the nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data transfers from the SRAM to the nonvolatile cell (the STORE operation) or from the nonvolatile cell to SRAM (the RECALL operation). All cells stored and recalled in parallel are enabled by this unique architecture. During the STORE and RECALL operations SRAM READ and WRITE operations are inhibited. The CY14B101L supports infinite reads and writes similar to a typical SRAM. It provides infinite RECALL operations from the nonvolatile cells and up to 200,000 STORE operations.

SRAM Read

The CY14B101L performs a READ cycle whenever \overline{CE} and \overline{OE} are LOW while \overline{WE} and \overline{HSB} are HIGH. The address specified on pins A_{0-16} determines which of the 131,072 data bytes are accessed. When the READ is initiated by an address transition, the outputs are valid after a delay of t_{AA} (READ cycle 1). If the READ is initiated by \overline{CE} or \overline{OE} , the outputs are valid at t_{ACE} or at t_{DOE} , whichever is later (READ cycle 2). The data outputs repeatedly respond to address changes within the t_{AA} access time, without the need for transitions on any control input pins. It remains valid until another address change or until \overline{CE} or \overline{OE} is brought HIGH, or \overline{WE} or \overline{HSB} is brought LOW.

SRAM Write

A WRITE cycle is performed whenever \overline{CE} and \overline{WE} are low and \overline{HSB} is high. The address inputs are stable before entering the WRITE cycle and must remain stable until either \overline{CE} or \overline{WE} goes high at the end of the cycle.

The data on the common IO pins IO_{0-7} are written into the memory if the data is valid t_{SD} before the end of a \overline{WE} controlled WRITE or before the end of an \overline{CE} controlled WRITE. Keep the \overline{OE} HIGH during the entire WRITE cycle to avoid data bus contention on common IO lines. If \overline{OE} is left LOW, internal circuitry turns off the output buffers t_{HZWE} after \overline{WE} goes LOW.

AutoStore Operation

The CY14B101L stores data to nvSRAM using one of the three storage operations:

1. Hardware Store activated by \overline{HSB}
2. Software Store activated by an address sequence
3. AutoStore on device power down

AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14B101L.

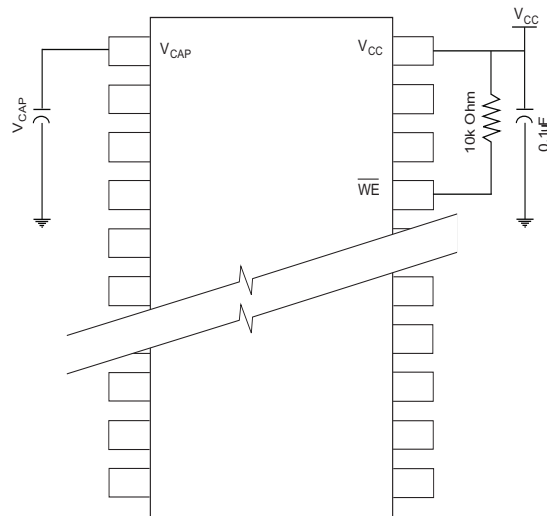
During normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH} , the part automatically disconnects the V_{CAP} pin from V_{CC} . A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Figure 3 on page 3 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to the

section DC Electrical Characteristics on page 6 for the size of V_{CAP} . The voltage on the V_{CAP} pin is driven to 5V by a charge pump internal to the chip. A pull up is placed on \overline{WE} to hold it inactive during power up.

To reduce unnecessary nonvolatile stores, AutoStore and Hardware Store operations are ignored unless at least one WRITE operation takes place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. Monitor the \overline{HSB} signal by the system to detect if an AutoStore cycle is in progress.

Figure 3. AutoStore Mode



Hardware STORE Operation

The CY14B101L provides the \overline{HSB} pin for controlling and acknowledging the STORE operations. Use the \overline{HSB} pin to request a hardware STORE cycle. When the \overline{HSB} pin is driven low, the CY14B101L conditionally initiates a STORE operation after t_{DELAY} . An actual STORE cycle only begins if a WRITE to the SRAM takes place since the last STORE or RECALL cycle. The \overline{HSB} pin also acts as an open drain driver that is internally driven low to indicate a busy condition while the STORE (initiated by any means) is in progress.

SRAM READ and WRITE operations that are in progress when \overline{HSB} is driven low by any means are given time to complete before the STORE operation is initiated. After \overline{HSB} goes LOW, the CY14B101L continues SRAM operations for t_{DELAY} . During t_{DELAY} , multiple SRAM READ operations take place. If a WRITE is in progress when \overline{HSB} is pulled LOW, it is allowed a time, t_{DELAY} to complete. However, any SRAM WRITE cycles requested after \overline{HSB} goes low are inhibited until \overline{HSB} returns HIGH.

During any STORE operation, regardless of how it is initiated, the CY14B101L continues to drive the \overline{HSB} pin LOW, releasing it only when the STORE is complete. After completing the STORE operation, the CY14B101L remains disabled until the \overline{HSB} pin returns high. Leave the \overline{HSB} unconnected if it is not used.

Hardware RECALL (Power Up)

During power up or after any low power condition ($V_{CC} < V_{SWITCH}$), an internal RECALL request is latched. When V_{CC} again exceeds the sense voltage of V_{SWITCH} , a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete.

Software STORE

Transfer data from the SRAM to the nonvolatile memory with a software address sequence. The CY14B101L software STORE cycle is initiated by executing sequential \overline{CE} controlled READ cycles from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. When a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence. If there are intervening READ or WRITE accesses, the sequence gets aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following READ sequence must be performed:

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x8FC0 Initiate STORE Cycle

The software sequence is clocked with \overline{CE} controlled READs or \overline{OE} controlled READs. When the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. It is important that READ cycles and not WRITE cycles are used in the sequence, although it is not necessary that \overline{OE} is low for the sequence to be valid. After the t_{STORE} cycle time is fulfilled, the SRAM is again activated for READ and WRITE operation.

Software RECALL

Transfer the data from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of \overline{CE} controlled READ operations must be performed:

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x4C63 Initiate RECALL Cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and then the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is again ready for READ and WRITE operations. The RECALL operation does not alter the data in the nonvolatile elements.

Table 2. Mode Selection

\overline{CE}	\overline{WE}	\overline{OE}	A15 – A0	Mode	IO	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	L	X	Read SRAM	Output Data	Active
L	L	X	X	Write SRAM	Input Data	Active
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active ^[1, 2, 3]
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active ^[1, 2, 3]

Notes

1. The six consecutive address locations are in the order listed. \overline{WE} is HIGH during all six cycles to enable a nonvolatile cycle.
2. While there are 17 address lines on the CY14B101L, only the lower 16 lines are used to control software modes.
3. IO state depends on the state of \overline{OE} . The IO table shown is based on \overline{OE} Low.

Table 2. Mode Selection (continued)

\overline{CE}	\overline{WE}	\overline{OE}	A15 – A0	Mode	IO	Power
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Store	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I_{CC2} ^[1, 2, 3]
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Recall	Output Data Output Data Output Data Output Data Output Data Output High Z	Active ^[1, 2, 3]

Preventing AutoStore

Disable the AutoStore function by initiating an AutoStore Disable sequence. A sequence of READ operations is performed in a manner similar to the software STORE initiation. To initiate the AutoStore Disable sequence, perform the following sequence of \overline{CE} controlled READ operations:

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x8B45 AutoStore Disable

Re-enable the AutoStore by initiating an AutoStore Enable sequence. A sequence of READ operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore Enable sequence, perform the following sequence of \overline{CE} controlled READ operations:

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual STORE operation (Hardware or Software) is issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled.

Data Protection

The CY14B101L protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low voltage condition is detected when V_{CC} is less than V_{SWITCH} . If the CY14B101L is in a WRITE mode (\overline{CE} and \overline{WE} LOW) at power up after a RECALL or after a STORE, the WRITE is inhibited until a negative transition on \overline{CE} or \overline{WE} is detected.

This protects against inadvertent writes during power up or brownout conditions.

Noise Considerations

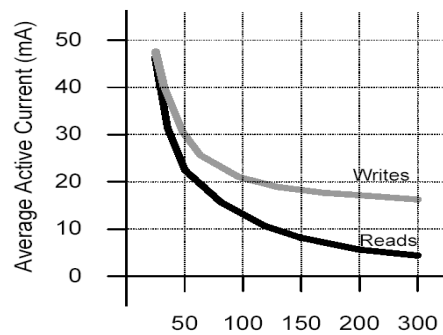
The CY14B101L is a high speed memory, and as a result, has a high frequency bypass capacitor of approximately 0.1 μ F connected between V_{CC} and V_{SS} , using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduces circuit noise.

Low Average Active Power

CMOS technology provides the CY14B101L the benefit of drawing less current when it is cycled at times longer than 50ns. Figure 4 shows the relationship between I_{CC} and READ/WRITE Cycle Time. Worst case current consumption shown for commercial temperature range V_{CC} is equal to 3.6V, and chip enable at maximum frequency. Only standby current is drawn when the chip is disabled. The overall average current drawn by the CY14B101L depends on the following items:

1. Duty cycle of chip enable
2. Overall cycle rate for accesses
3. Ratio of READs to WRITEs
4. Operating temperature
5. V_{CC} level
6. IO loading

Figure 4. Current vs. Cycle Time



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage on V _{CC} Relative to GND	-0.5V to 4.1V
Voltage Applied to Outputs in High Z State	-0.5V to V _{CC} + 0.5V
Input Voltage.....	-0.5V to V _{CC} + 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential	-2.0V to V _{CC} + 2.0V
Package Power Dissipation Capability (T _A = 25°C)	1.0W

Surface Mount Lead Soldering Temperature (three seconds)	+260°C
Output Short Circuit Current ^[4]	15 mA
Static Discharge Voltage.....	> 2001V (MIL-STD-883, method 3015)
Latch-up Current.....	> 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	2.7V to 3.6V
Industrial	-40°C to +85°C	2.7V to 3.6V

DC Electrical Characteristics

Over the Operating Range (V_{CC} = 2.7V to 3.6V) ^[5, 6, 7]

Parameter	Description	Test Conditions	Min	Max	Unit
I _{CC1}	Average V _{CC} Current	t _{RC} = 25 ns t _{RC} = 35 ns t _{RC} = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads. I _{OUT} = 0 mA.	Commercial	65 55 50	mA mA mA
I _{CC2}	Average V _{CC} Current during STORE	All inputs do not care, V _{CC} = Max Average current for duration t _{STORE}		6	mA
I _{CC3}	Average V _{CC} Current at t _{AA} = 200 ns, 3V, 25°C Typical	$\overline{WE} > (V_{CC} - 0.2)$. All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads. I _{OUT} = 0 mA.		10	mA
I _{CC4}	Average V _{CAP} Current during AutoStore Cycle	All inputs do not care, V _{CC} = Max Average current for duration t _{STORE}		3	mA
I _{SB}	V _{CC} Standby Current	$\overline{WE} > (V_{CC} - 0.2)$. All others V _{IN} < 0.2V or > (V _{CC} - 0.2V). Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.		3	mA
I _{IX}	Input Leakage Current	V _{CC} = Max, V _{SS} ≤ V _{IN} ≤ V _{CC}	-1	+1	μA
I _{OZ}	Off State Output Leakage Current	V _{CC} = Max, V _{SS} ≤ V _{IN} ≤ V _{CC} , \overline{CE} or $\overline{OE} > V_{IH}$	-1	+1	μA
V _{IH}	Input HIGH Voltage ^[7]		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage		V _{SS} - 0.5	0.8	V
V _{OH}	Output HIGH Voltage	I _{OUT} = -2 mA	2.4		V
V _{OL}	Output LOW Voltage	I _{OUT} = 4 mA		0.4	V
V _{CAP}	Storage Capacitor	Between V _{CAP} pin and V _{SS} , 5V rated	17	120	μF

Notes

- Outputs shorted for no more than one second. No more than one output shorted at a time.
- Typical conditions for the active current shown on the front page of the data sheet are average values at 25°C (room temperature) and V_{CC} = 3V. Not 100% tested.
- The HSB pin has I_{OUT} = -10 μA for V_{OH} of 2.4 V. This parameter is characterized but not tested.
- V_{IH} changes by 100 mV when V_{CC} > 3.5V.

Capacitance

These parameters are guaranteed but not tested.

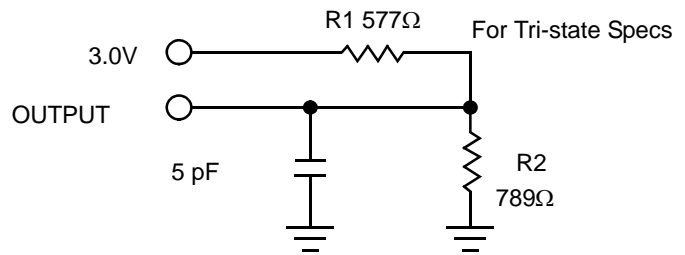
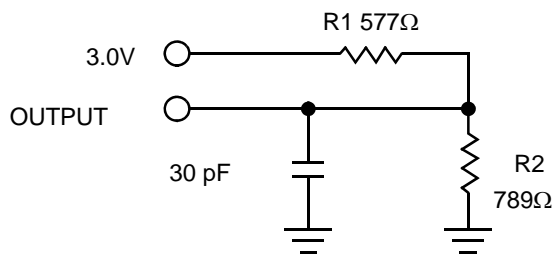
Parameter	Description	Test Conditions	Max	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 0 to 3.0 V	7	pF
C _{OUT}	Output Capacitance		7	pF

Thermal Resistance

These parameters are guaranteed but not tested.

Parameter	Description	Test Conditions	32-SOIC	48-SSOP	Unit
Θ _{JA}	Thermal Resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	TBD	TBD	°C/W
Θ _{JC}	Thermal Resistance (junction to case)		TBD	TBD	°C/W

AC Test Loads



AC Test Conditions

- Input Pulse Levels0V to 3V
- Input Rise and Fall Times (10% – 90%) ≤ 5 ns
- Input and Output Timing Reference Levels 1.5V

AC Switching Characteristics

Parameter		Description	25 ns Part		35 ns Part		45 ns Part		Unit
Cypress Parameter	Alt. Parameter		Min	Max	Min	Max	Min	Max	
SRAM Read Cycle									
t_{ACE}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
$t_{RC}^{[9]}$	t_{RC}	Read Cycle Time	25		35		45		ns
$t_{AA}^{[10]}$	t_{AA}	Address Access Time		25		35		45	ns
t_{DOE}	t_{OE}	Output Enable to Data Valid		12		15		20	ns
t_{OHA}	t_{OH}	Output Hold After Address Change	3		3		3		ns
$t_{LZCE}^{[11]}$	t_{LZ}	Chip Enable to Output Active	3		3		3		ns
$t_{HZCE}^{[11]}$	t_{HZ}	Chip Disable to Output Inactive		10		13		15	ns
$t_{LZOE}^{[11]}$	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
$t_{HZOE}^{[11]}$	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
$t_{PU}^{[8]}$	t_{PA}	Chip Enable to Power Active	0		0		0		ns
$t_{PD}^{[8]}$	t_{PS}	Chip Disable to Power Standby		25		35		45	ns
SRAM Write Cycle									
t_{WC}	t_{WC}	Write Cycle Time	25		35		45		ns
t_{PWE}	t_{WP}	Write Pulse Width	20		25		30		ns
t_{SCE}	t_{CW}	Chip Enable to End of Write	20		25		30		ns
t_{SD}	t_{DW}	Data Setup to End of Write	10		12		15		ns
t_{HD}	t_{DH}	Data Hold After End of Write	0		0		0		ns
t_{AW}	t_{AW}	Address Setup to End of Write	20		25		30		ns
t_{SA}	t_{AS}	Address Setup to Start of Write	0		0		0		ns
t_{HA}	t_{WR}	Address Hold After End of Write	0		0		0		ns
$t_{HZWE}^{[11, 12]}$	t_{WZ}	Write Enable to Output Disable		10		13		15	ns
$t_{LZWE}^{[11]}$	t_{OW}	Output Active after End of Write	3		3		3		ns

Notes

- 8. These parameters are guaranteed but not tested.
- 9. WE is HIGH during SRAM read cycles.
- 10. Device is continuously selected with CE and OE low.
- 11. Measured ± 200 mV from steady state output voltage.
- 12. If WE is low when CE goes low, the outputs remain in the high impedance state.

AutoStore or Power Up RECALL

Parameter	Description	CY14B101L		Unit
		Min	Max	
t _{HRECALL} ^[13]	Power Up RECALL Duration		20	ms
t _{STORE} ^[14, 15]	STORE Cycle Duration		12.5	ms
V _{SWITCH}	Low Voltage Trigger Level		2.65	V
t _{VCCRISE}	VCC Rise Time	150		μs

Software Controlled STORE/RECALL Cycles ^[16, 17, 18]

Parameter	Description	25 ns Part		35 ns Part		45 ns Part		Unit
		Min	Max	Min	Max	Min	Max	
t _{RC}	STORE/RECALL Initiation Cycle Time	25		35		45		ns
t _{AS}	Address Setup Time	0		0		0		ns
t _{CW}	Clock Pulse Width	20		25		30		ns
t _{GHAX}	Address Hold Time	1		1		1		ns
t _{RECALL}	RECALL Duration		50		50		50	μs
t _{SS} ^[19, 20]	Soft Sequence Processing Time		70		70		70	μs

Hardware STORE Cycle

Parameter	Description	CY14B101L		Unit
		Min	Max	
t _{DELAY} ^[21]	Time Allowed to Complete SRAM Cycle	1	70	μs
t _{HLHX}	Hardware STORE Pulse Width	15		ns

Notes

- 13. t_{HRECALL} starts from the time V_{CC} rises above V_{SWITCH}.
- 14. If an SRAM write has not taken place since the last nonvolatile cycle, no STORE takes place.
- 15. Industrial grade devices require 15 ms max.
- 16. The software sequence is clocked with \overline{CE} controlled or \overline{OE} controlled READs.
- 17. The six consecutive addresses are read in the order listed in the Table 2 on page 4. \overline{WE} is HIGH during all six consecutive cycles.
- 18. A 600Ω resistor must be connected to HSB to use the software command.
- 19. This is the amount of time it takes to take action on a soft sequence command. Vcc power remains HIGH to effectively register the command.
- 20. Commands such as STORE and RECALL lock out IO until operation is complete, which further increases this time. See the specific command.
- 21. READ and WRITE cycles in progress before HSB are given this amount of time to complete.

Switching Waveforms

Figure 5. SRAM Read Cycle 1 (address controlled) [9, 10, 22]

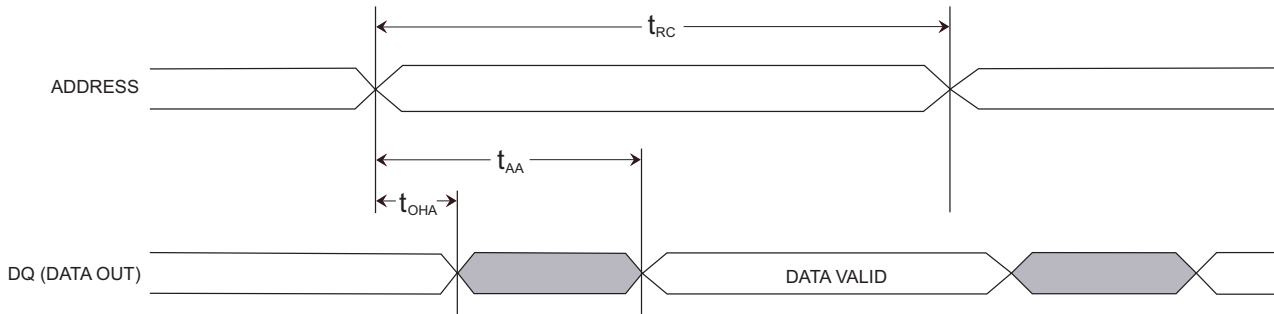
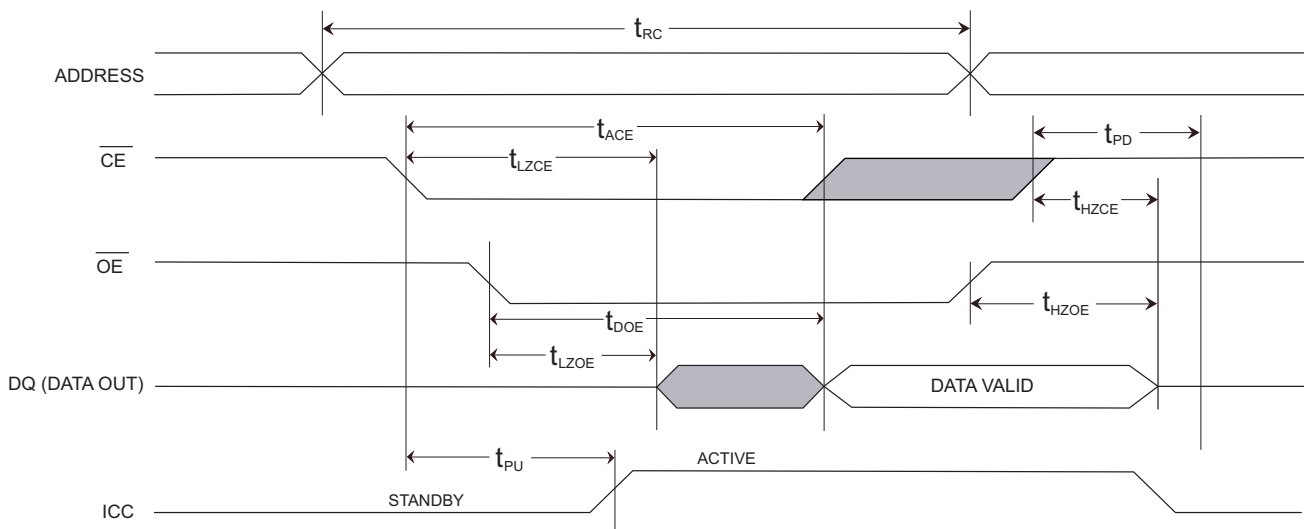


Figure 6. SRAM Read Cycle 2 (CE and OE controlled) [9, 22]



Note
22. HSB must remain HIGH during READ and WRITE cycles.

Switching Waveforms (continued)

Figure 7. SRAM Write Cycle 1 (WE controlled) [22, 23]

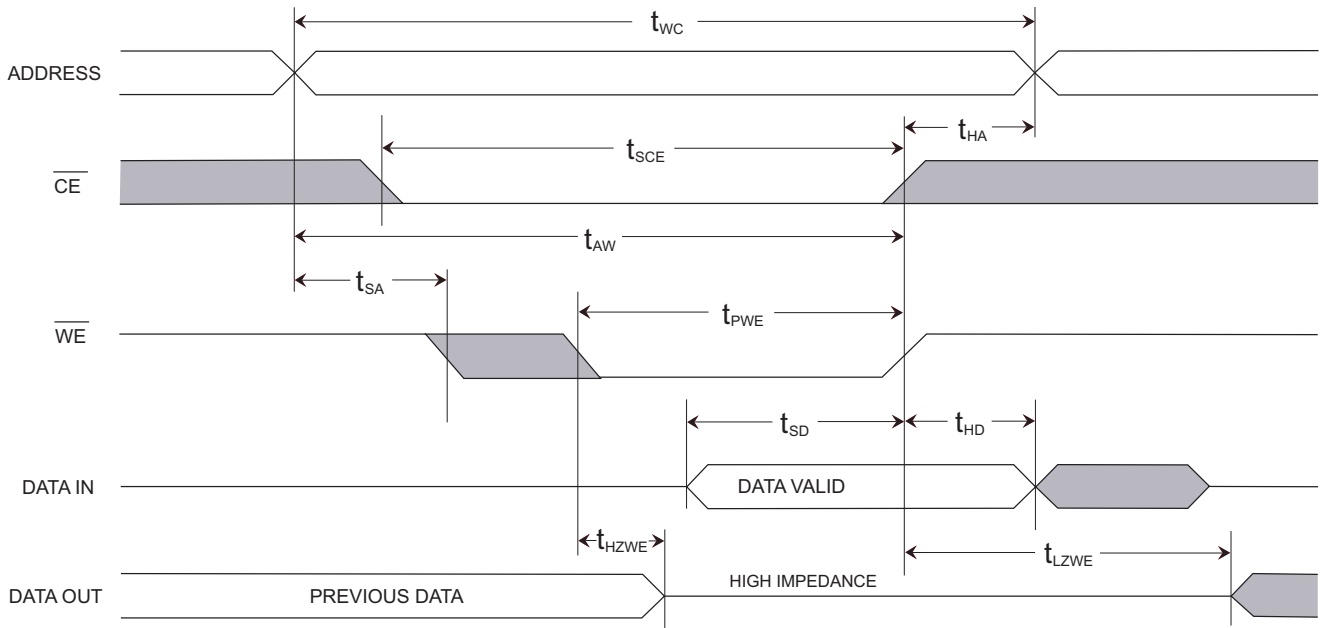
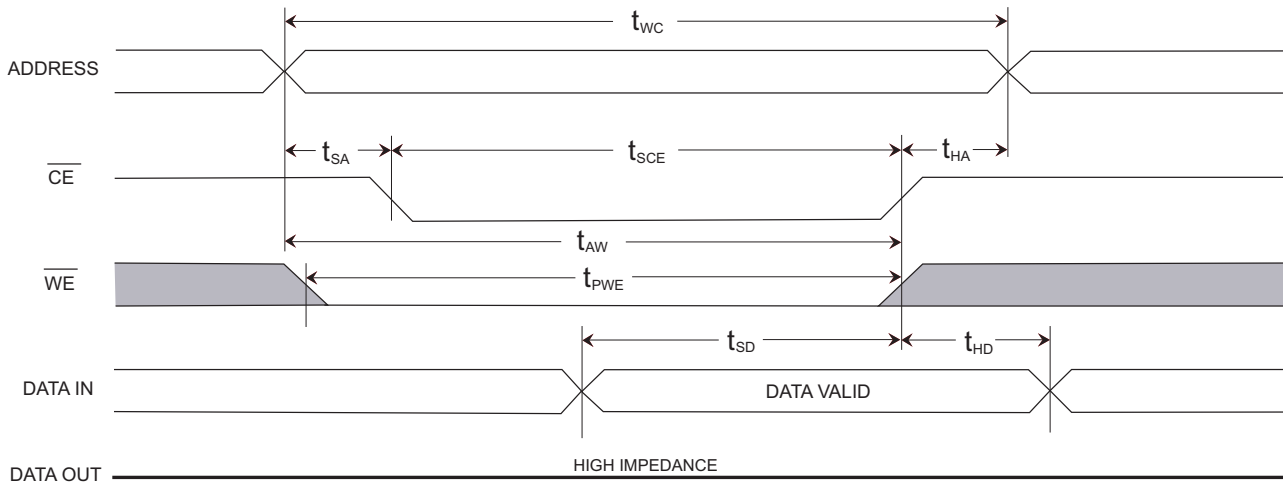


Figure 8. SRAM Write Cycle 2 (CE controlled)



Note
23. \overline{CE} or \overline{WE} must be $\geq V_{IH}$ during address transitions.

Switching Waveforms (continued)

Figure 9. AutoStore or Power Up RECALL

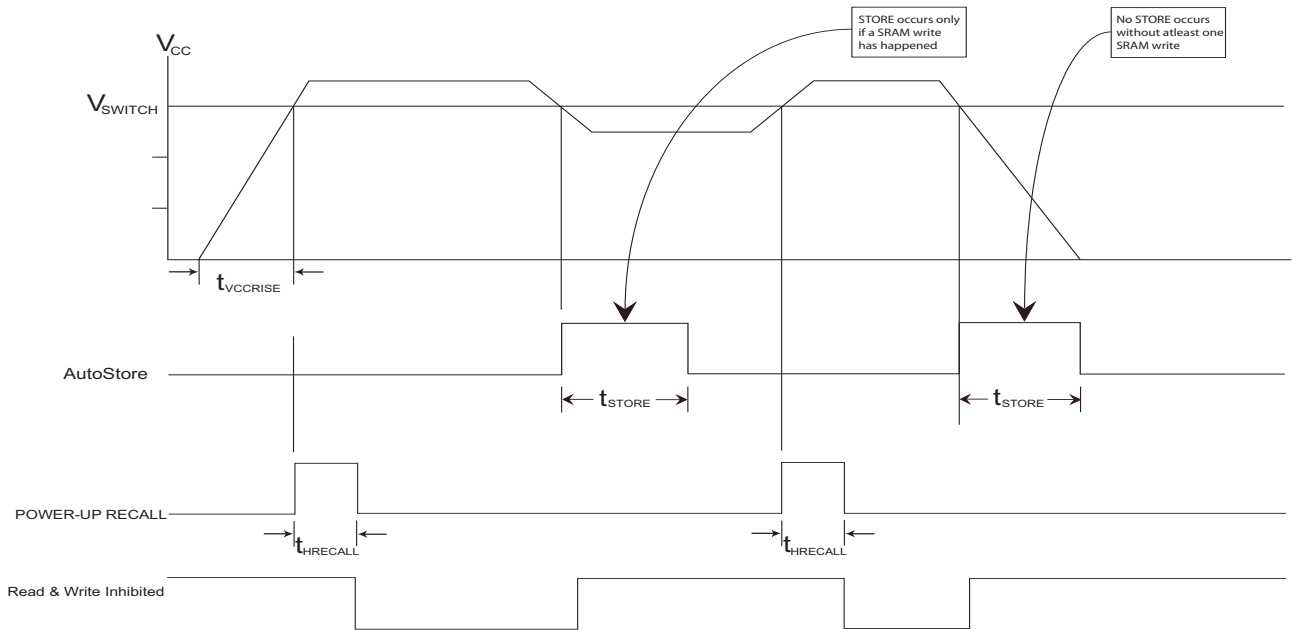
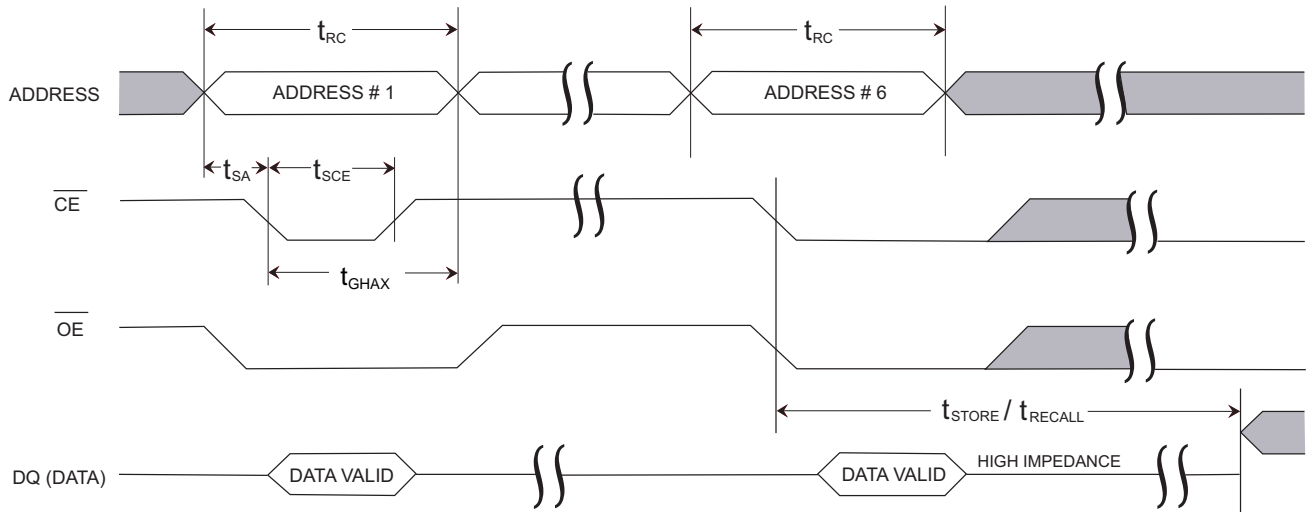


Figure 10. \overline{CE} Controlled Software STORE/RECALL Cycle [17]



Switching Waveforms (continued)

Figure 11. \overline{OE} Controlled Software STORE/RECALL Cycle [17]

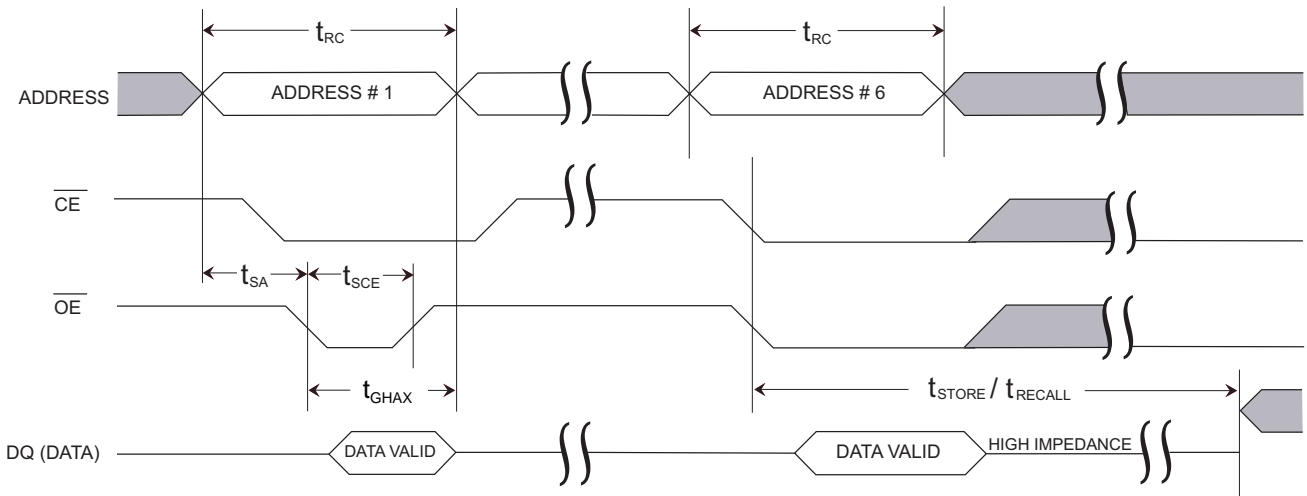


Figure 12. Hardware STORE Cycle

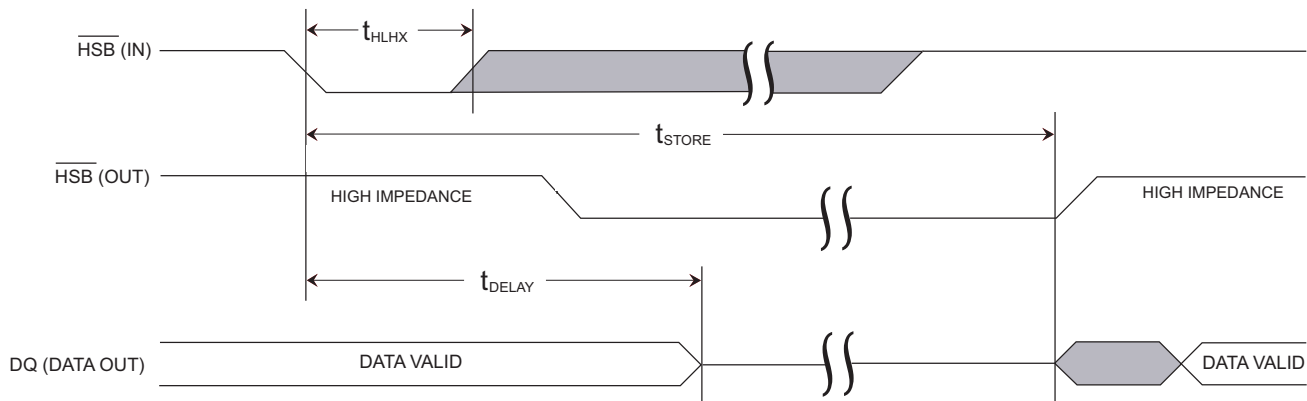
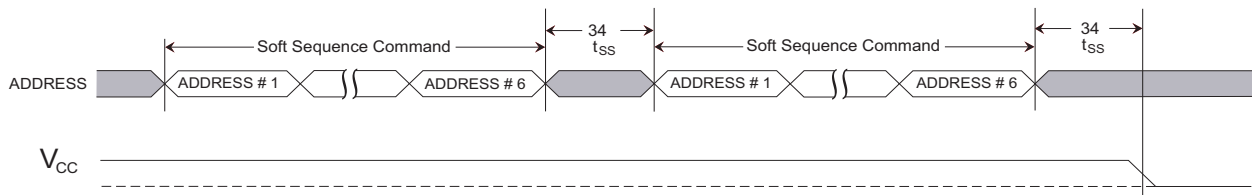
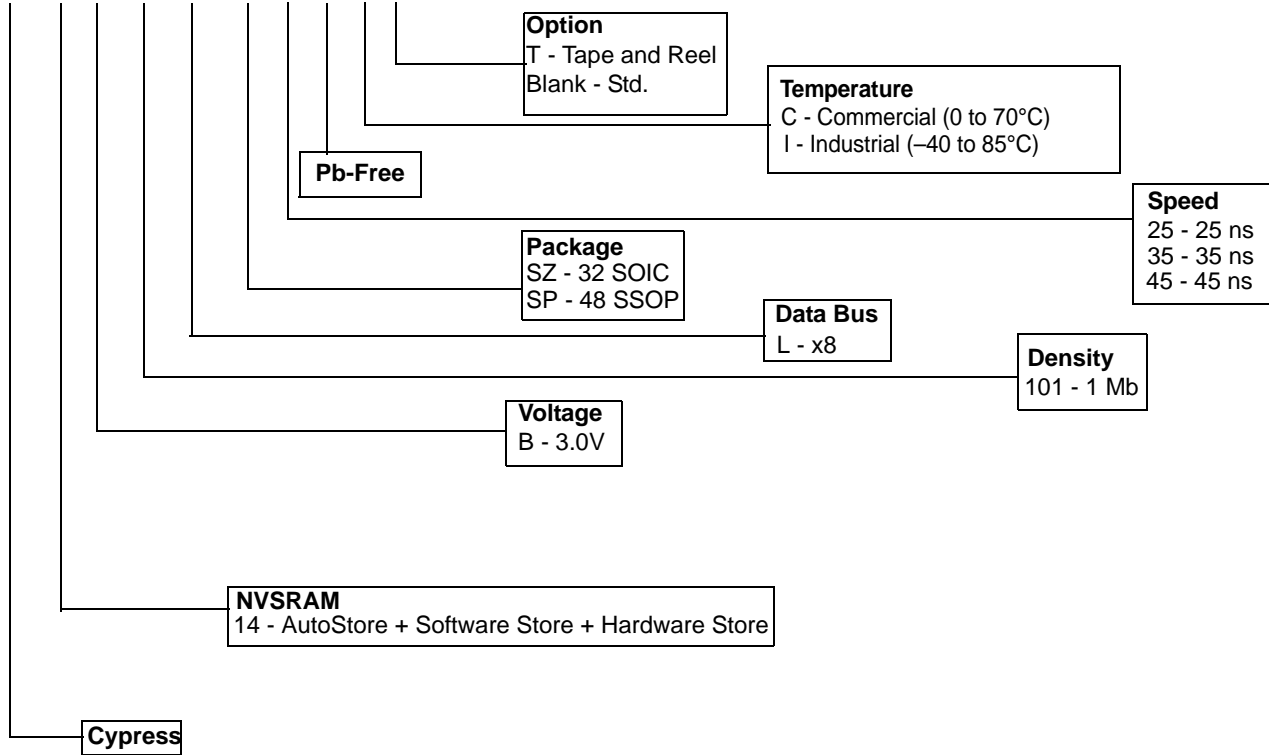


Figure 13. Soft Sequence Processing [19, 20]



Part Numbering Nomenclature

CY 14 B 101 L - SZ 25 X C T



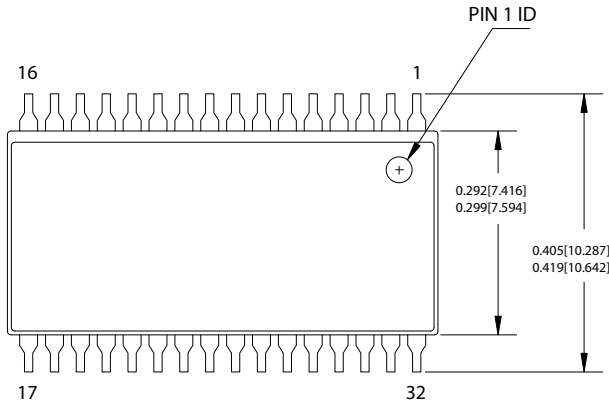
Ordering Information

The following parts are all Pb-free. Shaded areas contain advance information. Contact your local Cypress sales representative for availability of these parts.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY14B101L-SZ25XCT	51-85127	32-pin SOIC	Commercial
	CY14B101L-SP25XCT	51-85061	48-pin SSOP	
	CY14B101L-SZ25XC	51-85127	32-pin SOIC	
	CY14B101L-SP25XC	51-85061	48-pin SSOP	
25	CY14B101L-SZ25XIT	51-85127	32-pin SOIC	Industrial
	CY14B101L-SP25XIT	51-85061	48-pin SSOP	
	CY14B101L-SZ25XI	51-85127	32-pin SOIC	
	CY14B101L-SP25XI	51-85061	48-pin SSOP	
35	CY14B101L-SZ35XCT	51-85127	32-pin SOIC	Commercial
	CY14B101L-SP35XCT	51-85061	48-pin SSOP	
	CY14B101L-SZ35XC	51-85127	32-pin SOIC	
	CY14B101L-SP35XC	51-85061	48-pin SSOP	
35	CY14B101L-SZ35XIT	51-85127	32-pin SOIC	Industrial
	CY14B101L-SP35XIT	51-85061	48-pin SSOP	
	CY14B101L-SZ35XI	51-85127	32-pin SOIC	
	CY14B101L-SP35XI	51-85061	48-pin SSOP	
45	CY14B101L-SZ45XCT	51-85127	32-pin SOIC	Commercial
	CY14B101L-SP45XCT	51-85061	48-pin SSOP	
	CY14B101L-SZ45XC	51-85127	32-pin SOIC	
	CY14B101L-SP45XC	51-85061	48-pin SSOP	
45	CY14B101L-SZ45XIT	51-85127	32-pin SOIC	Industrial
	CY14B101L-SP45XIT	51-85061	48-pin SSOP	
	CY14B101L-SZ45XI	51-85127	32-pin SOIC	
	CY14B101L-SP45XI	51-85061	48-pin SSOP	

Package Diagrams

Figure 14. 32-Pin (300 Mil) SOIC

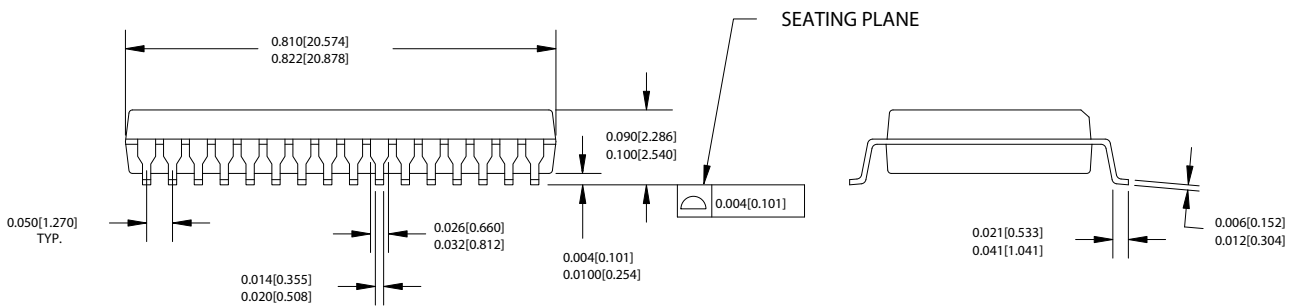


DIMENSIONS IN INCHES[MM]

MIN.
MAX.

REFERENCE JEDEC MO-119

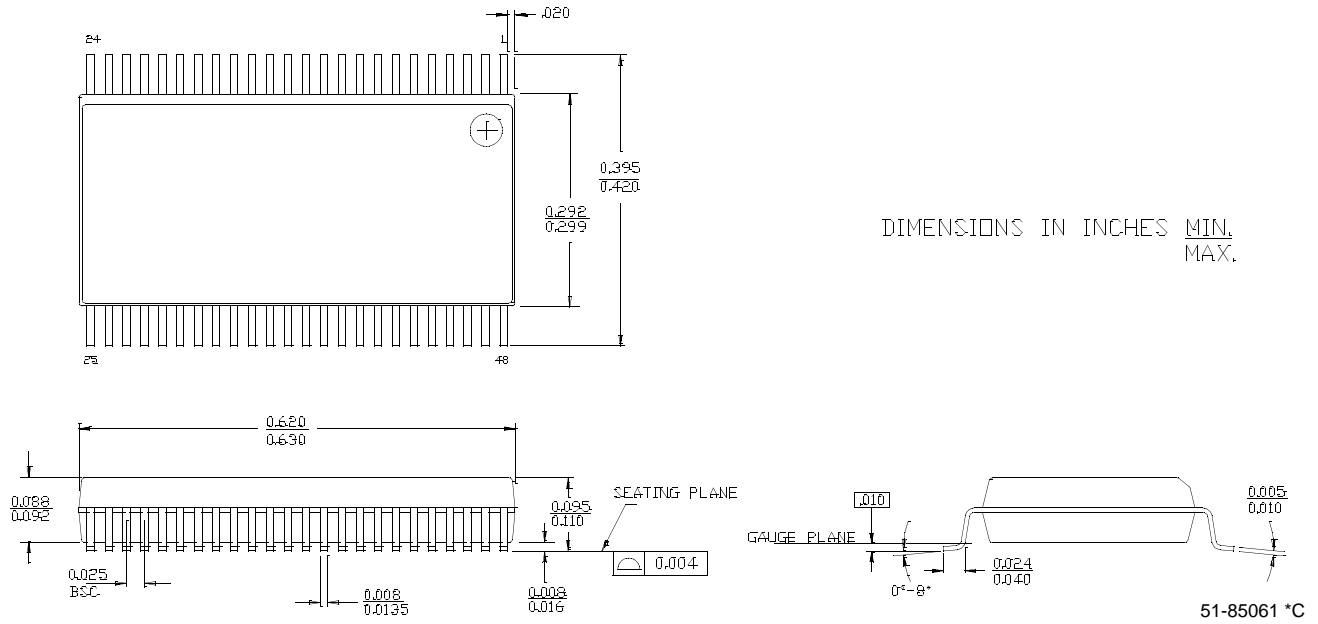
PART #	
S32.3	STANDARD PKG.
SZ32.3	LEAD FREE PKG.



51-85127 *A

Package Diagrams (continued)

Figure 15. 48-Pin Shrunk Small Outline Package



Document History Page

Document Title: CY14B101L 1 Mbit (128K x 8) nvSRAM				
Document Number: 001-06400				
REV.	ECN	Orig. of Change	Submission Date	Description of Change
**	425138	TUP		New data sheet
*A	437321	TUP		Show data sheet on External Web
*B	471966	TUP		Changed I _{CC3} from 5 mA to 10 mA Changed ISB from 2 mA to 3 mA Changed V _{IH(min)} from 2.2V to 2.0V Changed t _{RECALL} from 40 μs to 50 μs Changed Endurance from 1 million Cycles to 500K Cycles Changed Data Retention from 100 years to 20 years Added Soft Sequence Processing Time Waveform Updated Part Numbering Nomenclature and Ordering Information
*C	503272	PCI		Changed from Advance to Preliminary Changed the term "Unlimited" to "Infinite" Changed Endurance from 500K Cycles to 200K Cycles Added temperature specification to Data Retention - 20 years at 55°C Removed I _{cc1} values from the DC table for 25 ns and 35 ns industrial grade Changed I _{cc2} value from 3 mA to 6 mA in the DC table Added a footnote on V _{IH} Changed V _{SWITCH(min)} from 2.55V to 2.45V Added footnote 17 related to using the software command Updated Part Nomenclature Table and Ordering Information Table
*D	597002	TUP		Removed V _{SWITCH(min)} specification from the AutoStore/Power Up RECALL table Changed t _{GLAX} specification from 20 ns to 1 ns Added t _{DELAY(max)} specification of 70 μs in the hardware STORE cycle table Removed t _{HLBL} specification Changed t _{SS} specification from 70 μs (min) to 70 μs (max) Changed V _{CAP(max)} from 57 μF to 120 μF
*E	688776	VKN		Added footnote related to HSB Changed t _{GLAX} to t _{GHAX}
*F	1349963	UHA/SFV		Changed from Preliminary to Final Updated Ordering Information Table
*G	2427986	GVCH		Move to external web
*H	2546756	GVCH/AESA	08/01/2008	Aligned part number nomenclature Corrected typo in ordering information Changed pin definition of NC pin Updated data sheet template

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

PSoC	psoc.cypress.com
Clocks & Buffers	clocks.cypress.com
Wireless	wireless.cypress.com
Memories	memory.cypress.com
Image Sensors	image.cypress.com

PSoC Solutions

General	psoc.cypress.com/solutions
Low Power/Low Voltage	psoc.cypress.com/low-power
Precision Analog	psoc.cypress.com/precision-analog
LCD Drive	psoc.cypress.com/lcd-drive
CAN 2.0b	psoc.cypress.com/can
USB	psoc.cypress.com/usb

© Cypress Semiconductor Corporation, 2006-2008. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.